CLAIMS

1. A resistive structure integrated in a semiconductor substrate, comprising: a trench lined with dielectric material to form a dielectric trench; and a polysilicon region, at least a portion of which is doped, the polysilicon region completely surrounded by the dielectric trench so that the resistive structure is isolated electrically from other components jointly integrated in the semiconductor substrate, and wherein portions of the dielectric trench are formed with a plurality of trenches distributed about the polysilicon region to form a single dielectric region having a width that increases along the resistive structure in which a voltage drop increases.

2. The resistive structure of claim 1 wherein said polysilicon region and said dielectric region have a serpentine pattern, thereby reducing the space requirements of the resistive structure for a given resistance value.

3. The resistive structure of claim 2 wherein said serpentine pattern is formed to include rungs, said rungs are physically connected in parallel together by a metallization.

4. The resistive structure of claim 1 wherein said polysilicon region is masked and then etched to create a T-shaped structure providing connection paths of polysilicon.

5. The resistive structure of claim 1 wherein said polysilicon region comprises fill polysilicon that has been enhanced by implantation in its surface region only.

6. The resistive structure of claim 1, wherein said polysilicon region comprises two deposited layers of polysilicon, only a first of said layers being enhanced

by implantation to lower the values of parasitic capacitances associated with the resistive structure.

7. The resistive structure of claim 1, wherein said first polysilicon layer is enhanced by angled implantation and has a thickness dimension conforming to the sidewalls of the dielectric region to prevent said region from becoming filled completely.

8. The resistive structure of claim 1, wherein said semiconductor substrate is a SOI substrate and comprises a plurality of dielectric trenches between wells of integrated devices therein, and that doped polysilicon intended to form the resistive structure is introduced into said trenches, the resistive structure itself requiring no additional integration area.

9. An integrated resistive structure, comprising:

at least one trench formed in a semiconductor substrate to have a depth greater than a depletion region;

a dielectric layer formed of a dielectric oxide entirely coating all walls of the at least one trench; and

a polysilicon region filling the at least one trench to be isolated dielectrically from the semiconductor substrate, the polysilicon region having at least a portion that is doped.

10. The structure of claim 12 wherein the dielectric layer has vertical and horizontal dimensions that are greater than vertical and horizontal dimensions of the polysilicon region.

11. The structure of claim 9 wherein the polysilicon region has a T-shaped cross-sectional configuration with a stem portion filling the at least one trench

and a cap portion covering the at least one trench and overlapping a portion of a top surface of the silicon substrate on each side of the at least one trench.

12. The structure of claim 9 wherein the polysilicon region includes a doped surface region.

13. The structure of claim 9 wherein the polysilicon region comprises first and second layers of polysilicon, the second layer being undoped and the first layer implanted with a dopant.

14. The structure of claim 13 wherein the first layer of polysilicon is implanted by angled implantation and has a thickness dimension conforming to the walls of the dielectric-coated at least one trench to prevent complete filling of the at least one trench.

15. The substrate of claim 9, comprising a plurality of trenches coupled together electrically by metallization.

16. A resistive structure integrated in a semiconductor substrate, comprising:

a trench having a depth greater than a width and lined with dielectric material to form a dielectric trench, the dielectric trench formed with a plurality of trenches distributed to form a single dielectric region having a width that increases along the resistive structure where a voltage drop increases; and

a polysilicon region, at least a portion of which is doped, filling the dielectric trench to be surrounded by the dielectric material.

17. A resistive structure integrated in a semiconductor substrate, comprising:

a trench having a depth greater than a width and aligned with dielectric material to form a dielectric trench, the dielectric trench formed with a plurality of trenches distributed to form a single dielectric region having a width that increases along the resistive structure where a voltage drop increases; and

a polysilicon region filling the dielectric trench to be surrounded by the dielectric material, the polysilicon region comprising two deposited layers of polysilicon, only a first of the layers enhanced by implantation to lower the values of parasitic capacitances associated with the resistive structure.

18. A resistive structure integrated in a semiconductor substrate, comprising:

a trench lined with dielectric material to form a dielectric trench; and a polysilicon region, at least a portion of which is doped, the polysilicon region completely surrounded by the dielectric trench to electrically isolate the dielectric trench from other components jointly integrated in the semiconductor substrate, the polysilicon region formed to have a t-shaped structure providing connection paths of polysilicon.

19. The resistive structure of claim 18 wherein the polysilicon region and the dielectric region have a serpentine pattern, thereby reducing the space requirements of the resistive structure for a given resistance value.

20. The resistive structure of claim 19 wherein the serpentine pattern is formed to include rungs, said rungs are physically connected in parallel together by a metallization.

21. The resistive structure of claim 18 wherein the polysilicon region comprises fill polysilicon that has been enhanced by implantation in its surface region only.

22. The resistive structure of claim 18 wherein the polysilicon region comprises two deposited layers of polysilicon, only a first of said layers being enhanced by implantation to lower the values of parasitic capacitances associated with the resistive structure.

23. The resistive structure of claim 22 wherein the first polysilicon layer is enhanced by angled implantation and has a thickness dimension conforming to the sidewalls of the dielectric region to prevent said dielectric region from becoming filled completely.

24. The resistive structure of claim 18 wherein the semiconductor substrate is an SOI substrate and comprises a plurality of dielectric trenches between wells of integrated devices therein, and doped polysilicon introduced in the trenches.

25. The structure of claim 18 wherein the dielectric region is arranged to isolate the resistive structure formed in the process of oxidizing the sidewalls of the dielectric trench.

26. An integrated resistive structure, comprising:

at least one trench formed in a semiconductor substrate and having a depth greater than a depletion region;

a dielectric layer entirely coating all walls of the at least one trench; and

a polysilicon region filling the at least one trench to be isolated dielectrically from the semiconductor substrate, the polysilicon region having a t-shaped cross-sectional configuration with a stem portion filling the at least one trench and a cap

portion covering the at least one trench and overlapping a portion of a top surface of the silicon substrate on each side of the at least one trench, the polysilicon region having at least a portion that is doped.

27. An integrated resistive structure, comprising:

at least one trench formed in a semiconductor substrate;

a dielectric layer entirely coating all walls of the at least one trench; and

a polysilicon region comprising first and second layers of polysilicon filling the at least one trench, the second layer being undoped and the first layer implanted with a dopant.

28. The structure of claim 27 wherein the first layer of polysilicon is implanted by angled implantation and has a thickness dimension conforming to the walls of the dielectric-coated at least one trench to prevent complete filling of the at least one trench.